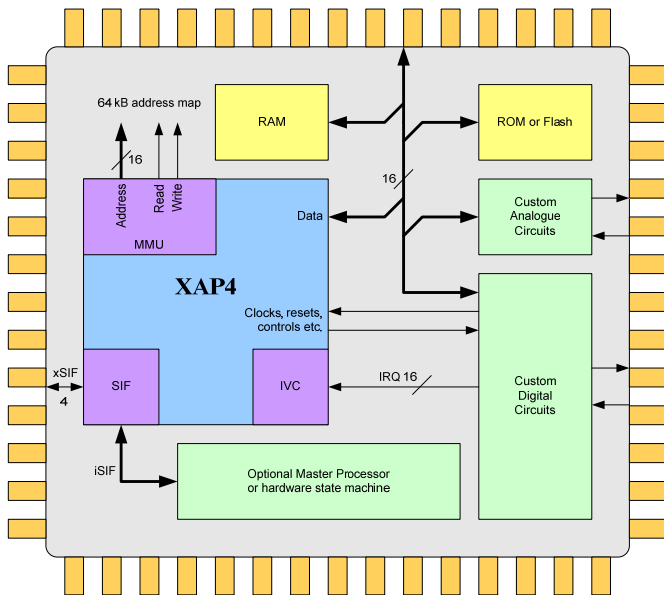


XAP4 processor core



XAP4 is a powerful 16-bit processor IP core with a modern architecture designed for use in ASIC devices such as sensors, implants, wireless or mobile products that demand high performance and high reliability coupled with low energy and a small footprint. This processor meets the requirements set by medical products, communication systems, sensors and new pervasive or ubiquitous computing applications.

At around 12k gates XAP4 is smaller than most other 16-bit and many 8-bit processors, and it consumes less energy. Yet it delivers a fast 0.95 DMIPS/MHz. XAP4 is an ideal replacement for 8-bit processors in projects requiring higher performance or reduced cost. It features excellent software portability and has very good code density, which saves program memory size and minimises die area and energy consumption.

Cambridge Consultants' XAP[®] family offers both 16- and 16/32-bit processors for a range of applications.

XAP4a features

- 16-bit, 64 kByte processor
- 16-bit registers: Eight general purpose, Program Counter, two Stack Pointers, Vector Pointer and two Breakpoints
- User mode and three privileged modes: Trusted, Supervisor, Interrupt
- 16 interrupts including two NMI
- 32 exception vectors
- Interrupt latency of 11 to 19 cycles
- Von Neumann architecture with little-endian organisation
- High code density – better than leading 32-bit processors
- Typical 65 nm routed area 0.029 mm²
- Core synthesis 12k gates (NAND2x1)
- 0.95 DMIPS/MHz from 16-bit memory
- Fast 285 DMIPS at 300 MHz*
- Very low power – 5 µW/MHz**
- High efficiency – 200 DMIPS/mW
- xSIF serial debug interface
- xIDE with GNU GCC C compiler
- Soft core, Verilog RTL delivery

Performance measured on 65 nm GP CMOS
 * Worst case 0.9 volt **Typical 1.0 volt

Low energy, low cost

XAP4 is the smallest core within Cambridge Consultants' family of powerful RISC processors, offering an efficient architecture and high-level programming environment.

A 16-bit XAP4 with 64 kB address capability offers adequate data precision and program size for many ASIC projects. It can often be used instead of a 32-bit core and memory, thus saving energy and silicon cost. 16-bit processors use fewer gates and a smaller RAM, thus reducing system size, cost and energy for a longer battery life.

XAP4's Von Neumann architecture simplifies design and memory management, especially for unified data and program memory systems running programs that are down-loaded into Flash memory.

The XAP4 processor is particularly efficient at running programs stored in Flash memory and its features support secure software updating and versatile in-place execution for lower memory cost and simplified software distribution.

Advanced architecture

XAP4 is a load-store machine with a regular instruction set for high code density, low bus traffic, easy decode, fast execution and good compilation. The instruction set is optimised for its native 16-bit data size and it also has instructions devoted to the efficient handling of single-bit and 8-bit data. 32-bit data is also supported by the processor hardware using pairs of registers.

Instruction fetch and execution is pipelined with most instructions executed in one or two cycles. Powerful multi-cycle instructions are included for fast performance.

XAP4's architecture, register set, instruction set and compiler are all designed for efficient execution of programs written in C, leading to high code density and reduced memory cost. The software tools include a GNU GCC C compiler, a Binutils assembler and source-level debugger. These tools are hosted in the xIDE software development environment, making the 16-bit XAP4 attractive to professional programming teams.

Sophisticated operation

XAP4 supports applications that must run with high reliability and high security. Software executes in User mode or one of the privileged modes: Trusted, Supervisor or Interrupt. The XAP4 will manage exceptions generated by a memory protection system that detects illegal code or data access.

XAP4 supports 16 interrupt and 32 exception events, each of which has its own handler accessed via a vector table. Processor hardware accelerates event handling and gives very fast interrupt response, even when interrupts are nested. There is also support for common operating system primitives such as atomic instructions for system synchronisation with semaphores. These features all provide XAP4 with the fast and deterministic performance that is required by applications using a pre-emptive Real-Time Operating System.

XAP4 uses a rich set of over 170 instructions that are represented in either 16- or 32-bit coding. The most common instructions are 16-bit, chosen for high code density. The linker optimises the run-time mix of instructions, which XAP4 executes irrespective of length.

Many instructions map closely to C language constructs in order to achieve very high code density and fast execution. There are multi-cycle instructions for block copy, block store, C function entry/exit, maths and DSP.

The XAP4 hardware includes good computation support; a single-cycle 32-bit shifter, a multi-cycle 16x16 multiplier and a 32/16 divider.

XAP4 uses unaligned memory access that simplifies porting code from other platforms. Unaligned data access and byte addressing store data efficiently in memory.

High performance

XAP4 is one of the best performing 16-bit processors available. The XAP4a has a two-stage pipeline for low cost, low energy applications, delivering a fast 0.95 Dhrystone MIPS per MHz. Combined with its high code density, this gives high performance at a low system cost.

This performance enables many applications to run code directly from a Flash memory thus saving on-chip RAM cost. For example, synthesised on a leading foundry's 65 nm CMOS logic (GP) process the XAP4a runs at 300 MHz, when it will achieve 285 Dhrystone MIPS. However, at 16 MHz it could run code directly from Flash memory and still deliver over 15 DMIPS.

Energy consumption can be minimised by operating the core at a reduced clock frequency. For example, at 1 MHz it consumes a miserly 5 μ W of dynamic power on the 65 nm process. For very low energy applications there is a sleep instruction that shuts the XAP down until a wake-up signal occurs.

Flexible implementation

XAP4a is a soft IP core written in Verilog RTL for synthesis to either ASIC or FPGA for verification. The core is implemented in around 12k gates including all of its registers. It can be laid out in a very small die area of under 0.03 mm² on 65 nm.

ASIC designers using XAP4 will customise its Memory Management Unit to interface their peripherals and memories, typically Flash and RAM, and also the Interrupt Vector Controller to prioritise interrupts and generate an interrupt vector.

XAP4 includes advanced features such as a Vector Pointer, Custom Logic Unit and iSIF interface. More details on these may be found in our data sheet for XAP5.

Reduced development risk

Real Time Operating Systems such as CMX, FreeRTOS and Micrium uC/OS-II are already ported to XAP4 with more to follow.

Debugging in real time with non-invasive access is facilitated by our patented xSIF serial interface included in all XAP processors.

The xIDE integrated development and debug environment provides a cross-platform software tool-chain for XAP4. It includes local variable debug and a XAP4 instruction set simulator. Python scripts can extend simulations to model other parts of an ASIC system, including peripherals and interrupts.

Application development can be accelerated using customised xIDE versions with software plug-ins that understand the ASIC. Cambridge Consultants can supply xIDE and plug-ins with a licensee's branding.

These tools combine to reduce risk and time-scale for XAP4 projects. Designers using them should get their ASIC right-first-time; even with programs stored in on-chip ROM, and a ROM patch mechanism can provide additional flexibility.

For applications requiring over 64 kBytes of memory use our 16/32-bit, 16 MByte XAP5 processor.

Visit our web site to discover how to apply for free 30-day trial copies of xIDE software tools for XAP.

XAP

www.CambridgeConsultants.com/XAP

This data sheet is for XAP architecture 4.2 available for sale (in confidence) from 28 Feb 2008: the data sheet was first published 10 July 2008.

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